Günhan Dündar

Department of Electrical and Electronic Engineering
Boğaziçi University
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Education

[1993] Ph.D., Electrical, Computer, and Systems Engineering
Rensselaer Polytechnic Institute, USA
Thesis: CMOS VLSI Design of Analog Neural Networks.

[1991] M.S., Electrical and Electronic Engineering
Boğaziçi University, Turkey.
Thesis: A Comparative Evaluation of Edge Detectors and Preprocessing Algorithms.

[1989] B.S., Electrical and Electronic Engineering
Boğaziçi University, Turkey.

Awards

The Vehbi Koç foundation award for the first 20 in the university entrance exam (1985-1989)

Boğaziçi University Research Fund Award (1996)

Boğaziçi University Foundation Encouragement Award (2000, 2001,2002,2003)

Boğaziçi University Foundation Young Researcher Award (2002)

Best Paper Award at the 19th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Leuven, Belgium. (2008)

TÜBİTAK Nationwide Encouragement Award (2009)

Elginkan Foundation Award for Research (2016)

Best Paper Runner up Award at the 13th IEEE International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lisbon, Portugal. (2016)

Experience

- 5/2002 – present: Full Professor, Boğaziçi University
- 4/2010 – 8/2010: Invited Professor, TUM.
- 9/2002 – 6/2003: Invited Professor, EPFL.
- 4/97 – 5/2002: Associate Professor, Boğaziçi University. Taught VLSI Design, Advanced VLSI Design, Computational VLSI, Electronic Circuits I and II, Electronics Laboratory, and Neural Networks.
- 6/96 – 4/97: Assistant Professor, Boğaziçi University. Taught a graduate course in computational VLSI and a second course in electronic circuits for junior level students.
- 1/94 - 6/96: Instructor, Boğaziçi University, Department of Electrical and Electronic Engineering. Taught graduate courses on microelectronic design, computational aspects of VLSI design, and semiconductor device theory. Taught undergraduate courses on introductory electronics for both electrical engineering and computer engineering students. Conducted electronic circuit labs.
- 11/94 - 12/95: Instructor, Naval Academy, taught Electronics Lab 1, Signals and Systems, Electronics Lab 2, and Digital Electronics.
- 8/94 - 12/95: Military service with the Turkish Navy.
- 1/94 - 6/94: Instructor, Air Force Academy, taught a course in Computer Networks.
- 7/90 - 7/91: Teaching Assistant, Boğaziçi University, Turkey. Held counseling hours for 5 junior/senior level courses on electronic circuits, digital electronic circuits and communication circuits. Instructed three electronics lab classes.
- 12/87 - 1/88: Trainee Engineer, Ekacomp, İstanbul. Worked in the servicing of microcomputers.
- 8/87 - 8/87: Trainee Engineer, Grundig, İstanbul.
- 6/87 - 8/87: Trainee Engineer, Philips, İstanbul. Worked in designing test benches for TV sets.

Areas of Research Interest

- Analog IC design
- Architectural modeling and circuit design of DSP and image processing systems.
- Design of analog neural networks
- Electronic design automation
- Image processing and data compression algorithms

Funded External Research Projects Conducted to Completion as the Project Coordinator

- Low Power consumption Sigma Delta A/D Converter Design, *for TÜBITAK (The Scientific and Technical Research Council of Turkey*), Project No:111E196, 2012-2016
- Design, realization and autmation of continuous time Sigma Delta A/D Converters, *for TÜBITAK (The Scientific and Technical Research Council of Turkey*), Project No:101E039, 2001-2004
- Continuous-time Bandpass Multi-Bit Sigma Delta Modulator, *for TÜBITAK (The Scientific and Technical Research Council of Turkey*) *and PIA (French agency)*, Project No:103E041, 2003-2005
- International Cooperation in Silicon Implementation of Computational Intelligence for Mechatronics, *for TÜBITAK (The Scientific and Technical Research Council of Turkey*) *and NSF,* Project No: 103E023, 2003-2005.
- A Design automation and modeling system for A/D Converters, *for TÜBITAK (The Scientific and Technical Research Council of Turkey*), Project No:105E028, 2005-2008
- Implementation of artificial neural networks with analog integrated circuits, *for TÜBITAK (The Scientific and Technical Research Council of Turkey*), Project No:EEEAG-183, 1996-1998.

Technical Training

- NATO ASI on Computational Intelligence, Turkey, August 1996.
- NATO ASI on System Level Synthesis, Italy, August 1998.
- RF Circuit Design for Wireless Communications, Switzerland, July 2000.

Administrative and Academic Services

- Member of the Curriculum, Faculty Search, PhD administration, and Technical Support Committees, Department of Electrical and Electronic Engineering, Boğaziçi University, (1998-present).
- Member of KOSGEB (Small Scale Industry Development Support) Evaluation Committee, Boğaziçi University, (1998-2010).
- Member of BİM (Computing Facilities) Committee (1998-2004), Boğaziçi University.
- Member of Boğaziçi University Press Committee (2004-present).
- Vice Chairman of the Electrical and Electronic Engineering Department, Boğaziçi University, (2003-2006, 2012-2014).
- Chairman of the Electrical and Electronic Engineering Department, Boğaziçi University, (2006-2009).
- Member of Boğaziçi University ÖYP Committee (2006 – present).
- Member of Boğaziçi University Foundation Academic Committee (2004-2007).
- Member of Boğaziçi University Teknopark (Technological Innovation Center) Evaluation Committee, (2012-2017).
- Member of Boğaziçi University Teknopark (Technological Innovation Center) Steering Committee, (2012-2017).

Memberships

- IEEE Member: Student Member (1989 – 1994), Member (1994 – 2013), Senior Member (2013 -)

Conferences Organized

- Turkish Artificial Intelligence and Neural Networks Symposium, June 1999 (TAINN 1999).
- PhD Research in Microelectronics and Electronics, June 2008 (PRIME 2008).
- The International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, September 2015 (SMACD 2015)

Seminars and Invited Talks

- G. Dündar: “ANNSyS – An Analog Neural Network Synthesis System”, University of Genoa, Genoa, Italy, August 1998.
- G. Dündar: “Non-idealities and component variations in analog neural networks”, Georgia Institute of Technology, Atlanta, Georgia, USA, August 1999.
- G. Dündar: “Design automation of analog integrated circuits”, EPFL, Lausanne, Switzerland, October 2002.

Courses to the Industry

- S. Balkır and G. Dündar: “Design Automation of Digital Circuits Using Mentor Graphics Software”, Havelsan, İstanbul, 1996.

M.S. Theses Conducted to Completion

- Top-down Design of CMOS Based Subsystems for DSP.
  Student: Hakan Binici, Co-advisor: Sina Balkır, Date: 1995.

- Circuit Simulation Based Training Algorithms for Analog Neural Networks.
  Student: İsmet Bayraktaroğlu, Co-advisor: Sina Balkır, Date: 1996.

- VLSI Implementation of a Neural Network Based Fuzzy Logic Controller.
  Student: Mustafa Sözer, Date: 1998.

- VLSI Implementation of a New Standard for Lossless Compression of Continuous Tone Still Images.
  Student: A. Suat Aktürk, Co-advisor: Sina Balkır, Date: 1998.

- Analog VLSI Implementation of Wavelet Transforms Using Switched Capacitor Filters.
  Student: Gürkan Sönmez, Co-advisor: Sina Balkır, Date: 1997.

- Amendment of Firing Mechanisms of Destructors Based on Development of Software and All Digital Circuitry.
  Student: İhsan Bakar, Co-advisor: Ömer Cerid, Date: 1997.

- Amendment of Firing Mechanisms of Destructors Based on Development of Hardware Solid State Sensors and All Analog Interfacing Circuitry.
  Student: Ayhan Bay, Co-advisor: Ömer Cerid, Date: 1997.

- ALG: An Analog Layout Generator.
  Student: Altuğ Şimşek, Co-advisor: Sina Balkır, Date: 1997.

- A Fast and Accurate Delay Estimation Method for Adders as CMOS Arithmetic Building Blocks in VLSI Design.
  Student: Gökhan Karakuş, Co-advisor: Sina Balkır, Date: 1998.

- An Optimized Method for the Estimation of Power Dissipation ın Adders as CMOS Arithmetic Building Blocks.
  Student: Arsal Dikel, Co-advisor: Sina Balkır, Date: 1998.

- Design of a High Resolution ADC.
  Student: Serhan Eröz, Co-advisor: Sina Balkır, Date: 1998.

- VLSI Implementation of a Secure Communication System Using Current-Mode Chaotic Circuits
  Student: Sedat Nişancı, Co-advisor: Sina Balkır, Date: 1999.

- Design of a Microcontroller Board and Development of Software for Ultrasonic Radar
  Student: Nilüfen Çotuk, Co-advisor: Ömer Cerid, Date: 1999.

- Hardware Implementation of Ultrasonic Radar System and Microcontroller Interfacing
  Student: Levent Bektaş, Co-advisor: Ömer Cerid, Date: 1999.

- Feedforward Neural Network Optimization Suitable for Hardware Implementation
  Student: Devrim Albuz, Date: 1999.

- Traffic Modeling in ATM Switches Using Neurofuzzy Methods
  Student: Amer Çatoviç, Co-advisor: Sema Oktuğ, Date: 1998.

- High-Level Synthesis of Analog Circuits
  Student: İ. Gökhan Erten, Co-advisor: Sina Balkır, Date: 1999.

- Performance Comparison of Viterbi Decoders
  Student: Levent Çetrez, Date: 2000.

- Performance Estimation in Analog CAD
  Student: İ. Faik Başkaya, Date: 2000.

- Theoretical Prediction of Parameter Quantization Effects in Gaussian Potential Function Neural Networks
  Student: Erkan Karakuş, Date: 2000.

- Architectures and Implementations for Speech Enhancement
  Student: Gökhan Coşgül, Date: 2000.

- Weight Quantization for Multilayer Perceptrons
  Student: Fatih Köksal, Co-advisor: Ethem Alpaydın, Date: 2000.

- Modeling of low noise FET amplifiers
  Student: Pınar Korkmaz, Date: 2000.

- Logic Level Power Estimation in CMOS VLSI Circuits
  Student: Mustafa Aktan, Date: 2001.

- A general design methodology for embedded high speed A/D converters
  Student: Selçuk Talay, Date: 2001.

- Design and Implementation of 3.2 Gbps LVDS Receiver
  Student: Erdem Karaadam, Date: 2002.

- VLSI implementation of a multiwavelet filter bank
  Student: Hakan Sunar, Date: 2002.

- Modeling mismatch between transistors on a wafer and the effect of mismatch in a CMOS GSM receiver
  Student: Özgür Ahmet Tarakçı, Date: 2002.

- Design and FPGA implementation of an STM-1 transceiver system containing the AES algorithm
  Student: Umut Yazkurt, Date: 2002.

- An Optimization-based Hierarchical Design Automation System
  Student: Öszun Serkan Sönmez, Date: 2003.

- An Analog Performance Estimation System Based on BSIM Models
  Student: Balkır Kayaaltı, Date: 2003.

- A flexible and high performance simulation based sensitivity analysis tool for analog layout constraint generation
  Student: Mehmet Selçuk Ataç, Date: 2003.

- A Single-chip solution for text-to-speech synthesis
  Student: Ozan Aktan, Date: 2004.

- Development of a library for CMOS analog neural networks
  Student: Mustafa Taşkaldıran, Date: 2004.

- Analog Design automation System “Performance Estimation”
  Student: Engin Deniz, Date: 2004.

- A Study of phase noise in differential CMOS LC Voltage Controlled Oscillators
  Student: Oktay Güryay, Date: 2004.

- An Analytical modeling approach to the design of PLL’s
  Student: Şeref Ersin Ak, Date: 2004.

- Analog Layout Generation
  Student: Ender Yılmaz, Date: 2006.

- Analog Design and Optimization of PWL circuits used in fuzzy logic solutions
  Student: Yankı Yalçın, Date: 2006.

- Power Analysis and Low Power Realization of Digital Filter Structures
  Student: Okan Zafer Batur, Date: 2006.

- Digital filter design, error modeling and error correction in sigma-delta modulators
  Student: Necmiye Genç, Date: 2007.

- High performance adaptive sigma delta modulator designs
  Student: Yiğit Dağhan Gökdel, Date: 2007.

- Implementation and performance evaluation of sigma-delta modulators
  Student: Muharrem Orkun Sağlamdemir, Date: 2007.

- Analog CMOS implementation of neuro-fuzzy systems
  Student: Baykal Sarıoğlu, Date: 2007.

- Yet another simulation based sensitivity analysis tool for analog layout generation
  Student: Taşkın Şen, Date: 2007.

- Current mode continuous time sigma delta converter design
  Student: Ufuk Yapar, Date: 2007.

- An automatic architecture generator for sigma-delta modulators considering component non-idealities
  Student: Ömer Yetik, Date: 2007.

- An efficient hardware implementation of the tate pairing in characteristic three
  Student: Giray Kömürcü, Co-advisor: Erkay Savaş, Date: 2008.

- 3.125Gbps FIR equalizer implementation in 65nm CMOS technology
  Student: Hande Akın Kurnaz, Date: 2008.

- Conversion of current mode continuous time sigma delta converters from 1 bit to 3 bits
  Student: Feyyaz Melih Akçakaya, Date: 2009.

- Sigma-delta dithering based frequency synthesis and modulation for DCS-1800
  Student: Oğuz Atasoy, Date: 2009.

- Analog circuit optimization with hierarchical genetic algorithms - 3rd order low-pass butterworth filter example
  Student: Olcay Durul Azeri, Date: 2009.

- Afronoc: an adaptive flexible network on chip router
  Student: Ömer Çoğal, Co-Advisor: Arda Yurdakul, Date: 2009.

- Power aware switched capacitor integrator design
  Student: Seyrani Korkmaz, Date: 2009.

- High performance adaptive sigma delta modulator designs
  Student: Sedef Kurşunoğlu, Date: 2009.

- Analog layout synthesizer for a parasitic aware design loop
  Student: Ahmet Unutulmaz, Date: 2009.

- Design of Blocks for an UWB Transceiver
  Student: Evren Akdağ, Date: 2010

- Second Order Sigma Delta Modulator Architecture with Low-Voltage Swing at the Output of First Integrator
  Student: Necmettin Levent Çakır, Date: 2010

- Power Optimization and Modeling of Switched Capacitor Integrators Suitable for Delta-Sigma Modulators
  Student: Gökhan Evci, Date: 2010

- Analog cell sizing using enhanced multi-objective evolutionary algorithm (MOEA/D-DE) and forming a feedback loop interface between SACSES and TOLAS
  Student: Süha Sipahi, Date: 2011

- An enhanced multi-objective evolutionary algorithm (MOEA/D-DE) for the applications of analog sizing with both W/L and a novel operating point driven (OPD) based methods
  Student: Murat Pak, Date: 2011

- Design of low power decimation filter for sigma-delta analog digital converters
  Student: Feyza Kayaduman, Date: 2011

- Integrated ultra-wideband receiver system and antenna design
  Student: Halit Kürşat Akkurt, Co-Advisor: Mutlu Koca, Date: 2011

- Aging in CMOS circuits and circuit design robust to aging phenomena
  Student: Engin Afacan, Co-Advisor: İ. Faik Başkaya, Date: 2011

- New approaches to optimization algorithms used in circuit and system levels of analog design automation
  Student: Simge Ay, Date: 2012

- Automatic sigma delta analog to digital converter architecture generator
  Student: Ali Murat Gök, Date: 2012

- Fast circuit topologies for finding the maximum of n k-bit numbers
  Student: Bilgiday Yüce, Co-Advisor: H. Fatih Uğurdağ, Date: 2013

- 10 bit 60 MS/s two step flash ADC design
  Student: Vahap Barış Esen, Date: 2013

- New approaches to automated analog circuit design for robustness
  Student: Can Doğa Kırbaç, Date: 2013

- Adaptive bias and class AB operational amplifier topologies for sigma delta converters
  Student: Tayyar Oğuz Karaduman, Date: 2013

- Design of low power continuous time analog to digital converters
  Student: Sina Parsnejad, Date 2014

- Low power continuous time sigma delta modulator and decimation filter design
  Student: Mehmet İnce, Date 2014

- An analog template router based on layout description script (LDS)
  Student: Cem Sümengen, Date: 2014

- Novel design methods for analog design automation tools
  Student: Gönenç Berkol, Date: 2015

- Design of high efficiency buck converters
  Student: Merve Toka Koç, Date: 2015

- Design and development of hall sensors for magnetic microsystems
  Student: Nazanin Takbiri, Date: 2015

- Design of a 12-Bit 3GS/s current steering DAC
  Student: Seyhan Çalışkan, Date: 2016

- Efficient yield estimation using rare event simulation techniques on analog design automation tools
  Student: Alphan Çamlı, Date: 2016

- Low power consumption continuous time sigma-delta modulator design
  Student: Hikmet Çeliker, Date: 2016

- Design of magnetic sensing microsystem with hall sensors
  Student: Ece Oktay, Co-advisor: Hamdi Torun, Date: 2016

- A 10 bit interface circuit for an array of capacitive transducers
  Student: Mohammad Ali Vosoughi, Co-advisor: Hamdi Torun, Date: 2016

PhD Theses Conducted to Completion

- A Silicon Compiler for Multirate DSP Systems
  Student: Arda Yurdakul, Co-advisor: Sabih Tansal, Date: 1999.

- Multilayer Perceptron Neural Networks in Analog VLSI – A System Level Study
  Student: A. Selçuk Öğrenci, Co-advisor: Sina Balkır, Date: 1999.

- A New Approach to Analog Integrated Circuit Optimization
  Student: Güner Alpaydın, Co-advisor: Sina Balkır, Date: 2000.

- Analysis and Modeling of Multi-gate MOSFET Structures
  Student: Koray Karahaliloğlu, Date: 2002.

- Hardware/Software Partitioning for Custom Instruction Processors
  Student: Kubilay Atasu, Co-Advisor: Can Özturan, Date: 2007

- High Level Power Efficient Synthesis of FIR Based Digital Systems
  Student: Mustafa Aktan, Date: 2008

- High Level Modeling of Sigma-Delta Analog to Digital Converters
  Student: Selçuk Talay, Date: 2008

- A Generalized Pareto Front Approach for Performance Estimation in Analog Design Automation Systems
  Student: Engin Deniz, Date: 2010

- Circuit Level Analog Design Automation
  Student: Özsun Serkan Sönmez, Date: 2010

- The design aspects of an optically powered CMOS receiver front-end for electrically isolated applications
  Student: Ozan Aktan, Date: 2011

- Realization and analysis of high performance physical unclonable functions based on ring oscillators
  Student: Giray Kömürcü, Co-advisor: Ali Emre Pusane, Date: 2014

- Ring oscillator based randon number generators
  Student: Ülkühan Güler, Date: 2014

- Design aspects of discrete time chaos based true random number generators
  Student: İhsan Çiçek, Date: 2014

- Enhanced layout-aware circuit / system synthesis
  Student: Ahmet Unutulmaz, Date: 2015

- Robust ultra-wideband tranceiver integrated circuit design
  Student: Okan Zafer Batur, Date: 2015

- Low power sigma delta analog to digital converter design methods
  Student: Feyyaz Melih Akçakaya, Date: 2016

- Analog circuit design automation against process variations and aging phenomena
  Student: Engin Afacan, Co-advisor: İ.F. Başkaya, Date: 2016

- Standard cell all-digital phase locked loop design, analysis and high-level synthesis
  Student: Yalçın Balcıoğlu, Date: 2016

Personal Information

Birth Place and Date: Istanbul, 1969
Marital Status: Married
Children: Two
Foreign Languages: English (fluent), German (medium), Italian (beginner), French (beginner).
Nationality: Turkish

Journal Publications

1. Y. Balcıoğlu and G. Dündar, "A standard cell phase locked loop design, analysis and high-level synthesis tool (CellPLL)," *Integration, the VLSI Journal*, Vol. 58, No. 6, pp. 142-154, June 2017.

2. Y. Balcıoğlu and G. Dündar, "A 0.65-1.35 GHz synthesizable all-digital phase locked loop with quantization noise suppressing time-to-digital converter," *Turkish Journal of Electrical Engineering & Computer Sciences*, Vol. 25, No. 3, pp. 2410-2423, 2017.

3. Ü. Güler, A. E. Pusane, and G. Dündar, "Design of efficient CMOS ring oscillator-based random number generator," *International Journal of Electronics*, Vol. 104, No. 9, 2017.

4. E. Afacan, G. Dündar, A.E. Pusane, M.B. Yelten, F. Başkaya, "Aging signature properties and an efficient signature determination tool for online monitoring," *Integration, the VLSI Journal*, Vol. 58, No. 6, pp. 496-503, June 2017.

5. İ. Çiçek, A.E. Pusane, and G. Dündar, "An Integrated Dual Entropy Core True Random Number Generator, " *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 64, No. 3, pp. 329-333, March 2017.

6. F.M. Akçakaya, G. Dündar, "Low power 3rd order feedforward sigma delta ADC design," *Turkish Journal of Electrical Engineering & Computer Sciences*, Vol. 25, No. 1, pp. 155-162, 2017.

7. B. Kayaaltı, Ö. Cerid, and G. Dündar, "A 0.18 um current-mode asynchronous sigma-delta modulator design," *Turkish Journal of Electrical Engineering & Computer Sciences*, Vol. 24, No. 6, pp. 4569 – 4581, December 2016.

8. M. Pak, F.V. Fernandez, and G. Dündar, "Comparison of QMC-based yield-aware pareto front techniques for multi-objective robust analog synthesis," *Integration, the VLSI Journal*, Vol. 55, No. 9, pp. 357-365, Sept. 2016.

9. E. Afacan, G. Berkol, G. Dündar, A.E. Pusane, and F. Başkaya, "A lifetime-aware analog circuit sizing tool," *Integration, the VLSI Journal*, Vol. 55, No. 9, pp. 349-356, Sept. 2016.

10. M.O. Sağlamdemir, G. Berkol, G. Dündar, A. Şen, "An analog behavioral equivalence boundary search methodology for simulink models and circuit level designs utilizing evolutionary computation, *Integration, the VLSI Journal*, Vol. 55, No. 9, pp. 366-375, Sept. 2016.

11. E. Afacan, G. Berkol, G. Dündar, A.E. Pusane, and F. Başkaya, "An analog circuit synthesis tool based on efficient and reliable yield estimation," *Microelectronics Journal*, Vol. 54, No. 8, pp. 14 -22, August 2016.

12. G. Kömürcü, A. E. Pusane, and G. Dündar, "Effects of aging and compensation mechanisms in ordering based RO-PUFs," *Integration, the VLSI Journal*, Vol. 52, pp. 71-76, 2016.

13. M.H. Mazaheri Kouhani, B. Çamlı, A.U. Çakacı, E. Kuşakçı, B. Sarıoğlu, G. Dündar, H. Torun, A.D. Yalçınkaya, "Integrated silicon photovoltaics on CMOS with MEMS module for catheter tracking," *Journal of Lightwave Technology*, Vol. 33, No. 16, pp. 3426 – 3432, 2015.

14. B. Sarıoğlu, M. Tümer, U. Çindemir, B. Çamlı, G. Dündar, C. Öztürk, and A.D. Yalçınkaya, "An Optically powered CMOS tracking system for 3 T magnetic resonance environment," *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 9, No. 1, pp. 12 – 20, February 2015.

15. A. Unutulmaz, G. Dündar, and F. V. Fernández, "On the convex formulation of area for slicing floorplans," *Integration, the VLSI Journal*, Vol. 50, pp. 74-80, 2015.

16. G. Kömürcü, A. E. Pusane, and G. Dündar, "An efficient grouping method and error probability analysis for RO-PUFs," *Computers and Security*, Vol. 49, pp 123-131, 2015.

17. G. Kömürcü, A.E. Pusane, and G. Dündar, "Enhanced challenge-response set and secure usage scenarios for ordering-based ring oscillator-physical unclonable functions," *IET Circuits, Devices & Systems,* Vol. 9, No. 2, pp. 87-95, 2015.

18. B. Sarıoğlu, M. Tümer, U. Çindemir, B. Çamlı, G. Dündar, C. Öztürk, A.D. Yalçınkaya, "An Optically powered CMOS tracking system for 3 T magnetic resonance environment," IEEE Transactions on Biomedical Circuits and Systems, Vol. 9, No. 1, pp. 12-20, 2015.

19. H. Torun, F.Ç. Top, G. Dündar, A.D. Yalçınkaya, "An antenna-coupled split-ring resonator for biosensing," *Journal of Applied Physics*, Vol. 116, pp. 124701, 2014.

20. B. Yüce, H.F. Uğurdağ, S. Gören, and G. Dündar, "Fast and efficient circuit topologies for finding the maximum of n k-bit numbers," *IEEE Transactions on Computers*, Vol. 63, No. 8, pp. 1868-1881, August 2014.

21. İ.Çiçek, A.E. Pusane, and G. Dündar, "A new dual entropy core true random number generator," *Analog Integrated Circuits and Signal Processing*, Vol. 81, No. 1, pp. 61 – 80, January 2014.

22. Ü. Güler and G. Dündar, "Modeling CMOS Ring Oscillator Performance as a Randomness Source," *IEEE Transactions on Circuits and Systems – I: Regular Papers*, Vol. 61, No. 3, pp. 712 – 724, March 2014.

23. E. Afacan, G. Dündar, and İ. F. Başkaya, "Reliability assessment of CMOS differential cross-coupled LC oscillators and a novel on chip self-healing approach against aging phenomena," *Microelectronics Reliability*, Vol. 54, No. 2, pp. 397-403, February 2014.

24. İ. Çiçek, A.E. Pusane, and G. Dündar, "A novel design method for discrete time chaos based true random number generators," *Integration, the VLSI Journal*, Vol. 47, No. 1, pp. 38-47, January 2014.

25. A Unutulmaz, G Dündar, F.V. Fernández, "Template coding with LDS and applications of LDS in EDA," *Analog Integrated Circuits and Signal Processing*, Vol. 78, No.1, pp. 137-151, January 2014.

26. G. Kömürcü, A.E. Pusane, and G. Dündar, "A Ring oscillator based PUF implementation on FPGA," *IU-Journal of Electrical & Electronics Engineering*, Vol. 13, No. 2, pp. 1647-1652, December 2013.

27. O.Z. Batur, E Akdağ, H.K. Akkurt, A Öncü, M Koca, G Dündar, "An Ultra Low-Power Dual-Band IR-UWB Transmitter in 130-nm CMOS," IEEE Transactions on Circuits and Systems – II, Vol. 59, No. 11, pp. 701 – 705, Nov. 2012.

28. K. Atasu, W. Luk, O. Mencer, C. Özturan, and G. Dündar, "FISH: Fast Instruction SynthHesis for Custom Processors," *IEEE Transactions on VLSI*, Vol. 20, No. 1, pp. 52-65, January 2012.

29. O. Aktan, B. Sarıoğlu, U. Çindemir, S. Ünlü, G. Dündar, Ş. Mutlu, and A. D. Yalçınkaya, "Optoelectronic CMOS Power Supply Unit for Electrically Isolated Microscale Applications," *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 17, No. 3, pp. 747 – 755, 2011.

30. Ö. S. Sönmez and G. Dündar, "Simulation-based analog and RF circuit synthesis using a modified evolutionary strategies algorithm," Integration, the VLSI Journal, Vol. 44, No. 22, pp. 144 – 154, 2011.

31. U. Yazkurt and G. Dündar, "DC-gain enhancement technique for differential current-mode integrators," *Electronics Letters*, Vol. 46, No. 11, pp. 750-752, 2010.

32. E. Yılmaz and G. Dündar, "Analog layout generator for CMOS circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***,** Vol.28, No. 1, pp. 32 – 45, January 2009.

33. S. Talay, E. Deniz, G. Dündar, "A Sigma-Delta ADC design automation tool with embedded performance estimator", *Integration – the VLSI Journal*, Vol. 42, No. 1, pp. 181 – 192, January 2009.

34. B.M. Wilamowski, N.J. Cotton, O. Kaynak, and G. Dündar, "Computing gradient vector and Jacobian matrix in arbitrarily connected neural networks," *IEEE Transactions on Industrial Electronics*, Vol. 55, No. 10, pp. 3784-3790, October 2008.

35. J.D. Hewlett, B.M. Wilamowski, and G. Dündar, "Optimization using a modified second-order approach with evolutionary enhancement," *IEEE Transactions on Industrial Electronics*, Vol. 55, No. 9, pp. 3374-3380, Sept. 2008.

36. M. Aktan, A. Yurdakul, and G. Dündar, "An algorithm for the design of low-power hardware efficient FIR filters," *IEEE Transactions on Circuits and Systems – I,* Vol. 55, No. 6, pp. 1536-1545, 2008.

37. K. Atasu, C. Özturan, G. Dündar, O. Mencer, and W. Luk, "CHIPS: Custom Hardware Instruction Processor Synthesis," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 27, No. 3, pp. 528-541, 2008.

38. K. Karahaliloğlu and G. Dündar, "An explicit current model for dual gate MOSFET," *Solid State Electronics,* Vol. 47, No. 11, pp. 2117-2125, 2003.

39. G. Alpaydın, S. Balkır, and G. Dündar, "An evolutionary approach to automatic synthesis of high performance analog integrated circuits," *IEEE Transactions on Evolutionary Computing*, Vol. 7, No. 3, pp. 240-257, 2003.

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