

Teaching MOS Integrated Circuit Amplifier Design to Undergraduates

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Abstract—The enhancement-mode MOSFET is the primary active device used in present-day digital and mixed-signal integrated circuit processes. Thus, it is important to introduce this device and associated circuit design methods early in the electronics curriculum. This article discusses four integrated circuit MOSFET amplifier configurations; the current source/active load stage, the source follower, the cascode connection, and the differential stage with a current mirror load. These stages serve as building blocks for more complex MOSFET amplifiers and allow the introduction of MOSFET integrated circuit design principles.

Index Terms—Active load stage, cascode connection, MOSFET amplifier.

I. INTRODUCTION

ELECTRONIC circuit design had its genesis in the vacuum tube era and continued to evolve through the discrete bipolar junction transistor era and through the BJT integrated circuit (IC) era. It has now entered the MOSFET IC era. Most analog and mixed-signal circuit design today is done on a CMOS bulk process, using enhancement mode devices that have very little relationship to their discrete MOSFET cousins.

The topic of analog electronic circuit design using MOSFET circuits fabricated in CMOS processes is typically reserved for a senior or graduate elective course in most university curricula [1], using a textbook intended for a graduate audience [2]. It is, however, important to include basic material on MOSFET IC design in the initial electronic circuit design course to prepare for the advanced course. Even in curricula that have limited electronic circuit design to a single required course, an appreciation for the principles involved in IC design should be imparted to the student.

Especially in programs that require only a single course, it is difficult to select topics that will be most important to the student. The need for completeness in electronics textbooks requires a breadth of coverage that makes it difficult to select the most appropriate material. The goal of this article is to suggest material that, when incorporated into the first electronic circuits course, can provide a fundamental design background in the MOSFET IC amplifier design area. Generally, breadth of coverage will be sacrificed in the basic course to include a meaningful coverage of this popular area.

The first suggestion is to clearly delineate to the student the differences between discrete and IC MOSFET circuit design.

These differences are covered in Section II. Next, some important building blocks that are currently important in the fabrication of MOSFET amplifiers are considered. A discussion of these building blocks allows design principles to be considered and also demonstrates the necessity of simulation in MOSFET design. Section III includes four different building blocks that may be used in larger MOS amplifier circuits. The effects of a small capacitive load and signal generator resistance on circuit performance are demonstrated through Spice simulations.

The succeeding material assumes the readers' familiarity with the MOSFET device and its simple small-signal or incremental equivalent circuit.

II. DIFFERENCES BETWEEN DISCRETE AND INTEGRATED CIRCUIT MOSFET DESIGN

One of the important differences between discrete and IC design is in the components selected to minimize chip area [3]. A resistor or capacitor typically occupies much more chip area than a transistor. If one of these two passive elements can be eliminated by using additional transistors, the circuit cost will be decreased. It is economical, for example, to replace load resistors found in discrete amplifiers with active loads, that is, other MOSFET's biased into the active region.

In addition, the ranges of values of both resistors and capacitors are limited in IC design. The large chip areas required for the fabrication of these elements in commonly used processes might limit resistor values to 50 k Ω and capacitor values to 50 pF or less. The size and number of these passive elements are then limited in order to conserve chip space. Large coupling capacitors, used so freely in discrete amplifiers, are unavailable in IC amplifiers.

Because the numbers of resistors and capacitors are minimized in IC design, amplifier configurations that differ from discrete configurations become more important. Of course, the differential stage [4], [5] is important, but so also are other less complex stages that should be considered in the first electronics class.

In discrete devices, the substrate is generally tied to the source inside the package. Most CMOS processes require that substrates be tied to the appropriate rails, that is, the nMOS substrate is tied to the most negative rail and the pMOS substrate is tied to the most positive. For those IC amplifier configurations having a source terminal that is not tied to a rail, the body effect must be considered.

Another difference is in the consideration of channel width in amplifier design. In MOSFET IC design, the selection of channel width is an integral part of the design procedure. This is

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not only different from MOSFET discrete design, but also differs from bipolar junction transistor IC design. The transconductance of a BJT depends on the dynamic base-emitter resistance which, in turn, depends on dc emitter current. It does not depend directly on dimensions. For a MOSFET, the channel width determines transconductance and is often critical to the design of the amplifier. For this reason, channel widths may vary from a value near the minimum channel length up to a factor of hundreds or even thousands times this length.

Another difference in IC design relates to the increased difficulty in modeling modern small channel length devices and the increased complexity of IC amplifiers. One result of this difference is that most amplifier circuits are so complex that they can be accurately analyzed only by simulation. Thus, simulation techniques become very important and should be integrated into the first electronics class to prepare for succeeding classes. Spice-based programs are imperative to demonstrate the interaction of various parameters with overall amplifier performance.

III. MOSFET IC AMPLIFIER CONFIGURATIONS

Some useful amplifier configurations or building blocks are

- 1) the common-source stage with current source load (active load stage),
- 2) the source-follower with current source load,
- 3) the cascode stage, and
- 4) the differential stage with current-mirror load.

Since present classes typically cover the operation of the simple current-mirror, a knowledge of this circuit is presumed before discussing the amplifier configurations mentioned.

A. Active Load Stage

A stage used often in IC design is the active load stage. Typically, the active load is a current source, based on the current mirror. The MOSFET active load stage might appear as in Fig. 1.

The pMOS current mirror provides bias current to the amplifying device, M1. This device sees a drain load that equals

$$R_{\text{out}} = r_{ds2} || r_{ds1}. \quad (1)$$

The midband voltage gain is now

$$A_v = -g_{m1} R_{\text{out}}. \quad (2)$$

The output capacitance for the amplifier of Fig. 1 is

$$C_{\text{out}} = C_{db1} + C_{db2} + C_{gd1} + C_{gd2} \quad (3)$$

giving an upper corner frequency of

$$f_{\text{high}} = \frac{(g_{ds1} + g_{ds2})}{2\pi(C_{db1} + C_{db2} + C_{gd1} + C_{gd2})}. \quad (4)$$

Of course, a load capacitance or input capacitance of a following stage will lower this value. An example will demonstrate the use of these equations and the manner in which a simulation can be related to the results.

Example: The current mirror of Fig. 1 supplies a current of $50 \mu\text{A}$ to the amplifying stage using values of $R = 80 \text{ k}\Omega$ and $V_{\text{DD}} = 5 \text{ V}$. The dc output voltage is adjusted by voltage source,

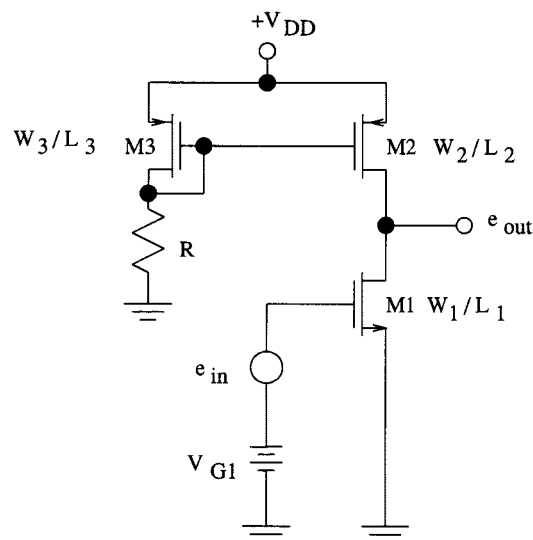


Fig. 1. A MOSFET stage with an active current source load.

V_{G1} , to be 2.4 V . If $g_{m1} = 0.19 \text{ mA/V}$, $g_{ds1} = 0.95 \mu\text{A/V}$, $g_{ds2} = 2 \mu\text{A/V}$, $C_{db1} = 11.0 \text{ fF}$, $C_{db2} = 32.0 \text{ fF}$, $C_{gd1} = 1.5 \text{ fF}$, and $C_{gd2} = 4.5 \text{ fF}$, calculate

- a) the midband voltage gain, A_v ;
- b) the upper corner frequency, f_{high} ;
- c) verify results with a Spice simulation.

Solution: The output resistance for this stage is

$$R_{\text{out}} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{10^6}{2.95} = 339 \text{ k}\Omega.$$

Using (2) leads to a voltage gain of

$$A_v = -g_{m1} R_{\text{out}} = -0.19 \times 10^{-3} \times 339 \times 10^3 = 64.4 \text{ V/V}.$$

The output capacitance is

$$\begin{aligned} C_{\text{out}} &= C_{db1} + C_{db2} + C_{gd1} + C_{gd2} \\ &= 11.0 + 32.0 + 1.5 + 4.5 = 49 \text{ fF}. \end{aligned}$$

From (4), this gives an upper corner frequency of

$$\begin{aligned} f_{\text{high}} &= \frac{1}{2\pi C_{\text{out}} R_{\text{out}}} \\ &= \frac{1}{2\pi \times 49 \times 10^{-15} \times 339 \times 10^3} = 9.58 \text{ MHz}. \end{aligned}$$

The Spice simulation file is listed in Table I.

This program uses a model for the MOSFETs named C5X.LIB. The results of this simulation are $A_v = -63.6 \text{ V/V}$ and $f_{\text{high}} = 8.53 \text{ MHz}$, which compare well with the calculated results.

In cascaded MOS stages, the load presented by the gate of a following stage is primarily capacitive. This is also the case for an output stage that connects to an IC pad and an output pin. Thus, it is important to see how a stage is affected when loaded with capacitance. Furthermore, the output resistance of a stage serves as the generator resistance to the following stage. It is important to note how gain and upper corner frequency depend on the generator resistance in series with the input of the stage.

TABLE I
SPICE FILE FOR EXAMPLE

```

EX11-1.CIR
R1 0 4 80K
V1 1 0 1.275V
V2 2 1 AC 0.005V
V3 5 0 5V
M1 3 2 0 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M2 3 4 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
M3 4 4 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
.AC DEC 10 100 10MEG
.OP
.PROBE
.LIB C5X.LIB
.END

```

The effect of a capacitive load or the effect of a generator resistance on the upper corner frequency and the voltage gain can be found by additional simulations.

The circuit of Fig. 1 is not driving a load. If this happens to be an output stage, its output will connect to an output pad of the IC chip. The capacitance associated with the pad might exceed 1 pF. If the simulation is repeated with a 1 pF load added, the upper corner frequency drops from 8.35 MHz to 431 kHz.

If this stage were loaded by a comparable stage rather than by 1 pF, the corner frequency might drop by a factor of two rather than a factor of 20. In order to avoid this drop, a buffer stage may be added to drive the 1 pF load without the large reduction in corner frequency.

Another possibility is to increase the values of W for all the devices. While this increases the capacitance, the output resistance decreases and g_m increases with W to result in a comparable voltage gain. The effect of the load capacitance on upper corner frequency will then be much less.

Another point relating to frequency response is that the simulated circuit is driven by a perfect voltage source with zero output resistance. If this stage were driven by an identical stage, the output impedance of the first stage would become the source resistance for the second stage. To demonstrate the effect of source resistance on upper corner frequency, a resistance of 339 k Ω is used as a source resistance for the circuit of Fig. 1. This particular value of resistance will be used in succeeding circuit examples for comparison purposes. No external load capacitance is used in this simulation. The simulated upper corner frequency is lowered in this situation from a value of 8.35 MHz to 3.08 MHz.

This value can also be calculated by noting that the input circuit will now cause a corner frequency determined by the source resistance and the input capacitance. The input capacitance equals the sum of C_{gs1} , C_{gb1} , and the Miller effect capacitance $(1 + |A|)C_{gd1}$. From the simulation, these values are

$$|A| = 63.6 \text{ V/V}, \quad C_{gs1} = 13.35 \text{ fF},$$

$$C_{gd1} = 1.5 \text{ fF}, \quad C_{gb1} = 0.3 \text{ fF}.$$

The total input capacitance resulting is approximately 111 fF. With a 339 k Ω source resistance, this adds a corner frequency

TABLE II
ANALYSIS RESULTS FOR ACTIVE LOAD STAGE

C_L , pF	R_S , k Ω	f_{high} , MHz
0	0	8.53
1	0	0.43
0	339	3.08
1	339	0.40

of

$$f_{in-high} = \frac{1}{2\pi C_{in} R_{in}} = 4.23 \text{ MHz}.$$

The amplifier now has an input corner frequency of 4.23 MHz and an output corner frequency of 8.53 MHz. An iterative method is used to calculate the overall upper corner frequency since two unequal single-poles determine the amplifier response. This results in a calculated overall corner frequency of $f_{high-calc} = 3.56$ MHz. This value exceeds the simulated value of 3.08 MHz by 15%.

If a source resistance of 339 k Ω and a 1-pF load capacitance are both added to the amplifier, the new upper corner frequency is found from simulation to be 399 kHz.

Table II summarizes the results of this analysis.

Generally, the capacitor values used in the manual calculations are found from the simulation that lists all parameter values at the bias point used.

This example demonstrates the use of an active load stage as well as the degrading effects of a capacitive load and a signal generator resistance. These effects must be understood in order to do effective IC design.

Approximate results are useful to provide a starting point for circuit simulations that are a necessity before an IC chip is laid out. Fabrication runs are very expensive, and mistakes must be avoided to minimize cost. Thus, the simulation step is never omitted in the IC design process. This step uses parameters for the MOS devices that are based on the actual process to be used in fabrication.

B. Source Follower with Active Load

The source follower provides a buffer stage, but the midband voltage gain is low, even less than the value of unity approached by the BJT emitter-follower stage. The bandwidth is quite high for the source-follower stage. Fig. 2 demonstrates a source follower with a current-mirror load.

The device M2 presents a resistance of r_{ds2} between the source of M1 and ground. In addition, device M1 presents a resistance of r_{ds1} in parallel with $1/g_{s1}$ between the source of this device and the dc power supply which is also ground for incremental signals. It should be noted that the body effect in M1 must be included since the source-to-substrate voltage of this device varies with the output signal. In fact, it equals the output signal.

The circuit of Fig. 2(b) is redrawn in Fig. 3 and the pertinent parasitic capacitances are added.

The two current sources $g_{m1}e_{out}$ and $g_{s1}e_{out}$ can be converted to conductances g_{m1} and g_{s1} , respectively. Fig. 4 shows an alternate equivalent circuit that is used to find the voltage gain as a function of frequency.

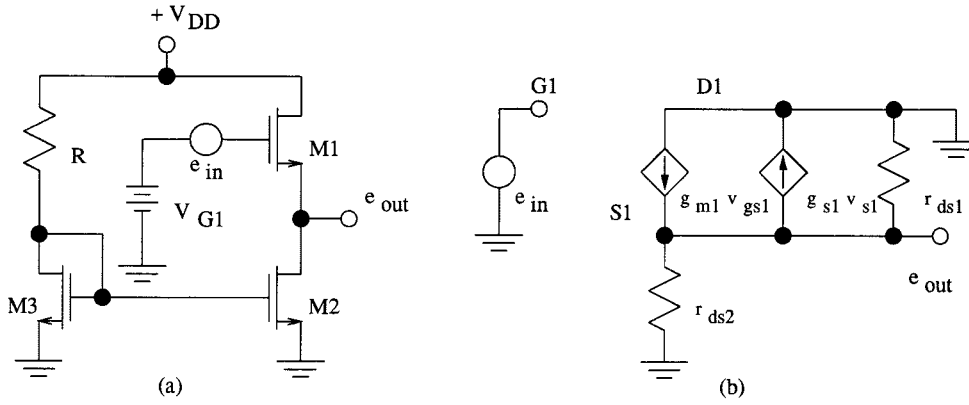


Fig. 2. (a) A source-follower stage with current source load. (b) Equivalent circuit.

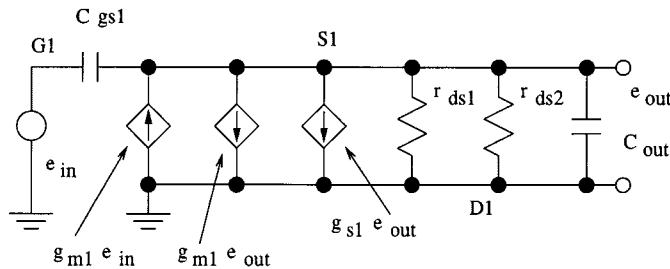


Fig. 3. The high-frequency source-follower equivalent circuit.

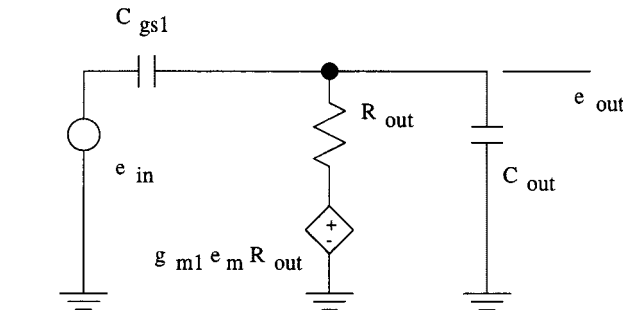


Fig. 4. Alternate equivalent circuit of the source follower.

The circuit of Fig. 4 is analyzed to find that

$$A(j\omega) = g_{m1}R_{out} \frac{\frac{j\omega C_{gs1}}{g_{m1}} + 1}{j\omega(C_{gs1} + C_{out})R_{out} + 1} \quad (5)$$

where

$$R_{out} = \frac{1}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} \quad (6)$$

and

$$C_{out} = C_{sb1} + C_{db2} + C_{gd2} \approx C_{sb1} + C_{db2}. \quad (7)$$

The midband gain can be evaluated by combining (5) and (6) and is

$$A_v = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} \quad (8)$$

In many submicron processes, the value of the denominator of (8) might equal 1.15 to 1.2 times g_{m1} . This leads to values of midband gain ranging from about 0.8 to 0.9 V/V.

The transfer function for voltage gain as a function of frequency shows a zero at

$$f_{zero} = \frac{g_{m1}}{2\pi C_{gs1}} \quad (9)$$

and a pole at

$$f_{pole} = \frac{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}}{2\pi(C_{gs1} + C_{out})}. \quad (10)$$

Typically, the zero frequency is higher than the pole frequency and the asymptotic frequency response appears as in Fig. 5.

At high frequencies the capacitor C_{gs1} feeds through from input directly to output causing a gain of

$$A_{high} = \frac{C_{gs1}}{C_{gs1} + C_{out}}. \quad (11)$$

In simulating a source-follower circuit with similar dimensions to those of the devices in the earlier example, the midband gain was found to be 0.81 V/V, and the upper corner frequency was 1.15 GHz. This was for a circuit with no input signal source resistance and no load capacitance. With a signal source resistance of 339 k Ω and a 1-pF load capacitance, the upper corner frequency becomes 37 MHz. This value is much higher than that of the common-source, active-load stage.

Useful principles to be stressed from the source-follower circuit are 1) the degrading effect on voltage gain of the nonzero voltage appearing at the source of the MOSFET and 2) the excellent frequency response of the circuit even in the presence of large capacitive loads.

As noted earlier, capacitive loading can be a serious problem for an output stage that connects to an IC pin which will connect to the input of another circuit. Because of the high output resistance of configurations such as the active load stage, a small capacitance of a pF or less will decrease the upper corner frequency significantly. The source follower stage is often inserted between a high-gain stage and the output pin of a chip to serve as a buffer stage. This buffer presents a rather low capacitance to the preceding stage since there is no Miller multiplication of C_{gd} and, as seen from the simulation, a 1 pF load capacitance can result in a reasonably high upper corner frequency.

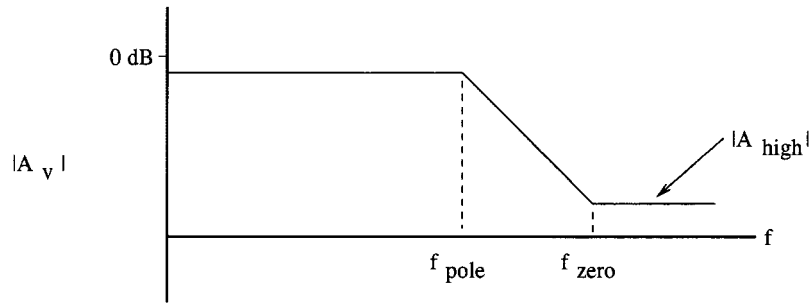


Fig. 5. Asymptotic frequency response of source follower.

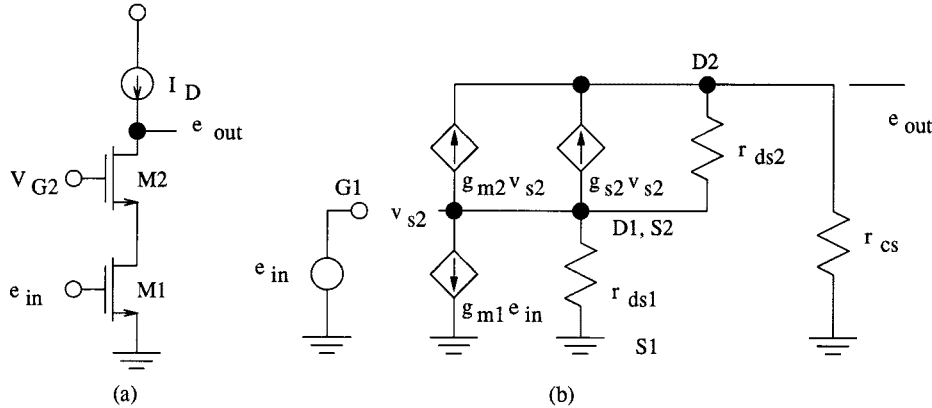


Fig. 6. (a) The MOSFET cascode amplifier stage. (b) Equivalent circuit.

C. The Cascode Connection

The cascode connection has been used for many years in high-frequency BJT circuits. It has become more important in IC MOSFET design in recent years. Fig. 6 shows the basic cascode circuit with a current source load.

The resistance r_{cs} is the output resistance of the current source. The equivalent circuit can be converted to a Thevenin circuit as shown in Fig. 7.

The output voltage is

$$v_{out} = -i r_{cs} \quad (12)$$

where i is the incremental drain current. Note that the upper voltage source is proportional to the source voltage of M2, v_{s2} . This voltage can be expressed as

$$v_{s2} = -g_{m1} r_{ds1} v_{in} - i r_{ds1}. \quad (13)$$

If the transconductance of M2 is added to the body effect transconductance, that is

$$g_{t2} = g_{m2} + g_{s2} \quad (14)$$

the midband voltage gain can be found to be

$$A_v = -\frac{(g_{m1} r_{ds1} + g_{t2} g_{m1} r_{ds1} r_{ds2}) r_{cs}}{r_{ds1} + r_{ds2} + r_{cs} + g_{t2} r_{ds1} r_{ds2}}. \quad (15)$$

This expression represents the product of two relatively large gains. As bias current decreases, the r_{ds} terms increase faster than the g_m terms decrease. Gains of several thousand can be

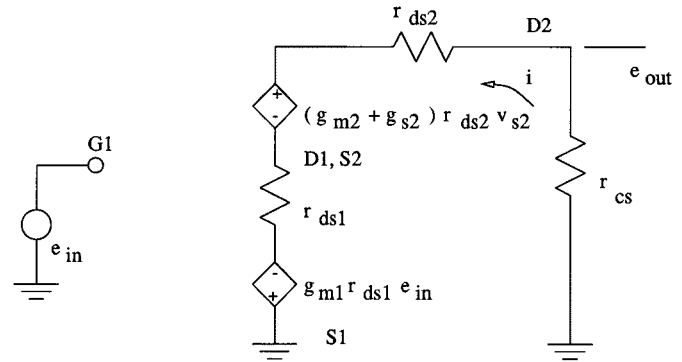


Fig. 7. An alternate equivalent circuit for the cascode.

obtained with this circuit. However, as r_{ds} increases, the high frequency response decreases, since the output resistance must drive the parasitic capacitance at the output of the stage.

A differential version of this stage is often used as an input stage in MOSFET op amp chips. A slightly different version of the cascode is the folded cascode that replaces M2 with a pMOS with a drain connection to ground [2]. The folded cascode stage will not be considered here.

The upper corner frequency of the cascode can be found from the equivalent circuit shown in Fig. 8.

The analysis of this circuit is somewhat complex. An accurate value can be found by simulation, but the upper corner frequency can be approximated rather easily. With no source resistance, the input capacitance will not influence the bandwidth. Also the corner frequency due to the capacitance C_1 will be affected by the parallel combination of r_{ds1} and the impedance,

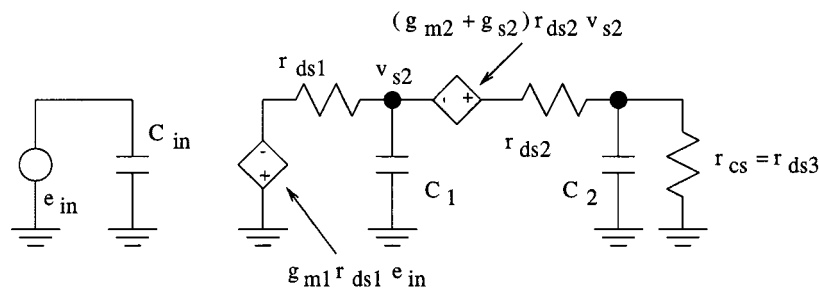


Fig. 8. High-frequency model of the cascode.

R_{s2} , looking into the source of M2. This impedance will be much less than r_{ds1} and can be approximated by

$$R_{s2} = \frac{1}{g_{m2} + g_{s2}}. \quad (16)$$

This corner frequency will be quite large, at least compared to that caused by C_2 . The resistance seen by this capacitance is $r_{ds3} || R_{out2}$ where r_{ds3} is the output impedance of a simple current mirror, and R_{out2} is the impedance looking into the drain of M2. This latter impedance will be quite large since the source resistance of M2 equals r_{ds1} . This output resistance of M2 will be very high; thus, the resistance seen by C_2 is approximately r_{ds3} . The upper corner frequency of the cascode can then be approximated by

$$f_{high} = \frac{1}{2\pi r_{ds3} C_2} \quad (17)$$

where $C_2 = C_{db2} + C_{gd2} + C_{db3} + C_{gd3}$.

A simulation with all dc drain currents at 50 μA results in $A_v = -46.9 \text{ V/V}$ and $f_{high} = 9.65 \text{ MHz}$. In order to demonstrate the effect of current on gain and bandwidth, the circuit is simulated for a drain current of 10.7 μA . For this situation, the simulated results are $A_v = -94.1 \text{ V/V}$ and $f_{high} = 2.52 \text{ MHz}$. The gain has approximately doubled while the bandwidth has dropped by a factor of about 4.

If a source resistance is present, a second corner frequency is added at the input due to C_{in} of Fig. 8. When a 339 k Ω source resistance is added to the cascode circuit with $I_D = 50 \mu\text{A}$, the new upper corner frequency is 8.95 MHz, representing a relatively small change from the original value of 9.65 MHz. This result implies that C_{in} is rather small. It should be emphasized for the cascode connection that the input capacitance is small since the Miller effect is minimized by a small voltage gain from gate to drain of M1.

If a load capacitance of 1 pF is added, but no source resistance is present, the upper corner frequency is lowered to 552 kHz. Adding the source resistance to this circuit leads to no further reduction of the upper corner frequency.

D. The Differential Connection with Current Mirror Load

This stage is significant in that it preserves the good common-mode rejection properties of the double-ended output differential stage, but produces a single-ended output signal. Fig. 9 shows a block diagram of such an arrangement.

With no input signal applied to the differential stage, the tail current splits equally between I_{diff1} and I_{diff2} . The input current to the mirror then equals $I_{tail}/2$. This value is also mirrored to

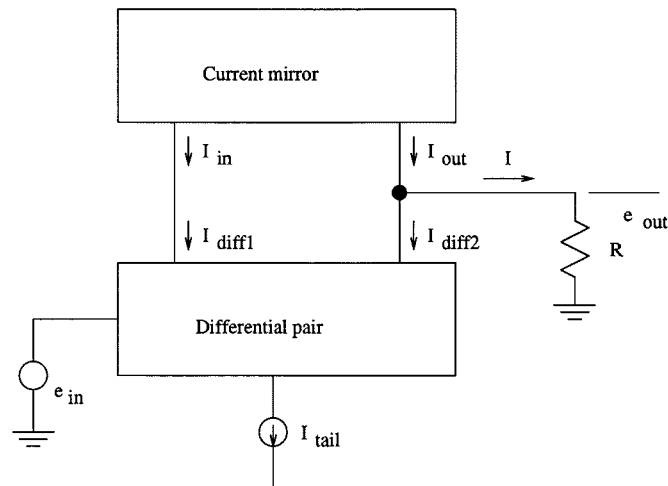


Fig. 9. Differential pair with current mirror load.

the output of the mirror giving $I_{out} = I_{tail}/2$. It is assumed that the voltage between the current mirror output and the second differential stage is approximately zero, although this assumption is unnecessary to achieve the correct result.

When a signal is applied to the differential input, it may increase the current I_{diff1} by a peak value of ΔI . The input current to the mirror now becomes

$$I_{in} = \frac{I_{tail}}{2} + \Delta I. \quad (18)$$

The output current from the mirror also equals this value. However, the input signal to the differential stage will decrease I_{diff2} by the same amount that I_{diff1} increases. Thus, we can write

$$I_{diff2} = \frac{I_{tail}}{2} - \Delta I. \quad (19)$$

The current to the resistance R increases from its quiescent value of zero to

$$I = I_{out} - I_{diff2} = 2\Delta I. \quad (20)$$

The incremental output voltage resulting is then

$$e_{out} = 2R\Delta I. \quad (21)$$

When an incremental input signal is applied to the differential pair, half of this voltage will drop across each gate-source terminal pair. The gate-source voltages result in equal incremental differential stage currents in the two output devices, but these

currents will be in opposite directions. An incremental input signal, e_{in} , will produce incremental currents of

$$i_{diff1} = \Delta I = \frac{g_m e_{in}}{2} \quad (22)$$

and

$$i_{diff2} = -\Delta I = -\frac{g_m e_{in}}{2} \quad (23)$$

where g_m is the transconductance of devices 1 and 2.

Assuming negligibly large output resistances of the current mirror and the differential stage, the incremental output voltage becomes

$$e_{out} = 2i_{diff1}R = g_m R e_{in} \quad (24)$$

with a resulting gain of

$$A_D = g_m R. \quad (25)$$

If the output resistances of the mirror and differential stage are significant, they can be combined in parallel with the load resistance to use in (25). The load resistance may, in fact, be the small-signal input resistance of the following stage. Very large values of voltage gain can result from this configuration.

While this expression is the same as that for the differential gain of a resistive load stage, two significant points should be made. First of all, the impedance R can be much greater than any resistive load that can be used in a differential stage. Large values of R in the differential stage would cause saturation of the stages for reasonable values of tail current. The current mirror solves this problem. The second point is that the output voltage of the differential pair with a current mirror load is a single-ended output which can be applied to a following simple amplifier stage. However, the rejection of common-mode variables caused by such factors as temperature change is still in effect with the current mirror stage. If a resistive load stage must provide a single-ended output, the gain drops by a factor of 2 and common-mode rejection no longer takes place.

IV. CONCLUSION

This article suggests a means of teaching MOSFET IC design in the first electronic circuit design course. The proposed circuit configurations represent several useful single-stage amplifiers encountered in IC design. A consideration of these amplifier building blocks can serve as the vehicle to convey principles of

IC circuit design and prepare students for more advanced circuit design courses.

The importance of simulation in circuit design can be demonstrated by simulating the operation of several of the building block circuits. Modifications in loading of the input and output circuits emphasize the utility of simulation programs.

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